AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please renumber claims 21-23 as claims 20-22.

Please cancel claim 10 with out prejudice.

1. (CURRENTLY AMENDED) A semiconductor device comprising:

at least one fixed memory block implemented with one or more diffused memories;

at least one R-cell memory block implemented in one or more diffused regions; and

control logic (i) implemented in said one or more diffused regions and (ii) configured to couple said at least one R-cell memory to said at least one fixed memory block, wherein said one or more diffused regions are ~~configurable~~ configured to ~~provide~~ expand one or more ports ~~for~~ of said ~~one or more diffused memories~~ at least one fixed memory block.

2. (CURRENTLY AMENDED) The semiconductor device according to claim 1, wherein said one or more diffused regions are ~~customizable~~ customized in response to designer specifications.

3. (CURRENTLY AMENDED) The semiconductor device according to claim 2, wherein said diffused regions are ~~customizable in response to~~ customized by placing one or more

metalization layers on said diffused regions based upon said designer specifications.

4. (CURRENTLY AMENDED) The semiconductor device according to claim 1, wherein said one or more diffused regions are ~~configurable~~ configured to ~~provide~~ couple a port of said at least one fixed memory block to a plurality of clock domains.

5. (CURRENTLY AMENDED) The semiconductor device according to claim 1, wherein said one or more diffused regions are ~~configurable~~ configured to ~~provide~~ expand one or more ports for said one or more diffused memories.

6. (CURRENTLY AMENDED) The semiconductor device according to claim 1, wherein said one or more diffused regions comprise a plurality of R-cells, each R-cell comprising one or more transistors or gates that are customized by placement of one or more metal layers.

7. (CURRENTLY AMENDED) The semiconductor device according to claim ~~6~~1, wherein said ~~R-cells~~ diffused regions are customized to provide one or more first-in-first-out (FIFO) memories.

8. (CURRENTLY AMENDED) The semiconductor device according to claim 7, wherein said ~~R-cells~~ diffused regions are further customized to provide control logic associated with said one or more FIFO memories.

9. (ORIGINAL) The semiconductor device according to claim 7, wherein each of said one or more FIFO memories are configured as one of an input buffer and an output buffer for at least one of said one or more diffused memories.

10. (CANCELED)

11. (CURRENTLY AMENDED) The semiconductor device according to claim ~~10~~1, wherein said at least one fixed memory block comprises one or more of (i) a one port, single read, single write (111) memory, (ii) a two ports, single read, single write (211) memory and (iii) a two ports, two reads, two writes (222) memory.

12. (CURRENTLY AMENDED) The semiconductor device according to claim ~~10~~1, wherein said at least one R-cell memory block comprises one or more of (i) a two ports, single read, single write (211) memory and (ii) a two ports, two reads, two writes (222) memory.

13. (CURRENTLY AMENDED) The semiconductor device according to claim ~~10~~1, wherein said semiconductor device comprises a structured application specific integrated circuit.

14. (CURRENTLY AMENDED) A semiconductor device comprising:

means for implementing at least one fixed memory block using one or more diffused memories; and

means for implementing ~~a plurality of ports for~~ at least one ~~of said~~ R-cell memory block and associated control logic using one or more diffused ~~memories~~ regions, wherein said at least one R-cell memory and associated control logic are configured to expand a single port of said fixed memory block into a plurality of ports ~~are implemented using R-cells~~.

15. (CURRENTLY AMENDED) A method for laying out a semiconductor device comprising the steps of:

~~providing~~ implementing at least one fixed memory block using one or more diffused memories; and

~~providing~~ implementing at least one R-cell memory block and associated control logic using one or more diffused regions comprising R-cells, wherein said at least one ~~or more diffused regions comprising R-cells are~~ R-cell memory and associated ~~with~~

~~said one or more diffused memories~~ control logic are configured to expand a single port of said fixed memory block into a plurality of ports.

16. (ORIGINAL) The method according to claim 15, further comprising the step of:

customizing said one or more diffused regions comprising R-cells with one or more metal layers.

17. (CURRENTLY AMENDED) The method according to claim 15, further comprising the step of:

~~implementing~~ configuring said at least one R-cell memory block as one or more FIFO memories associated with one or more clock domains ~~in said one or more diffused regions comprising R-cells~~.

18. (CURRENTLY AMENDED) The method according to claim 17, further comprising the step of:

associating said one or more FIFO memories with ~~a~~ said single port of said at least one ~~of said one or more diffused memories~~ fixed memory block.

19. (CURRENTLY AMENDED) The method according to claim 18, further comprising the steps of:

~~implementing~~ configuring said control logic ~~in~~ implemented using said one or more diffused regions comprising R-cells~~, wherein said control logic is configured~~ to couple said one or more FIFO memories to said single port.

20. (ORIGINAL) The method according to claim 15, wherein said one or more diffused memories comprise one or more of (i) a one port, single read, single write (111) memory, (ii) a two ports, single read, single write (211) memory and (iii) a two ports, two reads, two writes (222) memory.

21. (CURRENTLY AMENDED) The method according to claim ~~21~~15, further comprising the step of:

customizing said one or more diffused regions comprising R-cells to implement one or more R-cell memory blocks selected from the group ~~comprising one or more~~ consisting of (i) a two ports, single read, single write (211) memory and (ii) a two ports, two reads, two writes (222) memory.

22. (CURRENTLY AMENDED) The method according to claim ~~22~~21, further comprising the step of:

coupling at least one of said one or more diffused memories with said one or more R-cell memory blocks implemented in said one or more diffused regions comprising R-cells.